ZBT CONFIDENTIAL

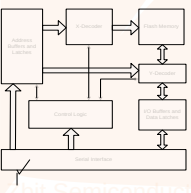
ZBT CONFIDENTIAL

The ZB25VQ128 support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripheral Interface (QPI): Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (WP#), and I/O3 (HOLD# / RESET#). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O and QPI instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The E(o6i-3((o)-(ou-6(o))4(us)-3( )-Read(on)4(22(Mo)3n)4(d)e0(8)-2

The

ZBIT CONFIDENTIAL

ZBT CONFID


Address Buffers and Latches
X-Decoder
Y-Bank Memory
Y-Decoder
Control Logic
I/O Buffers and Data Latches
Serial Interface

4. SIGNAL DESCRIPTIONS

Table 4.1 Pin Descriptions

Symbol	Pin Name
CLK	Serial Clock Input
DI(IO0)	Serial Data Input(Data input output 0) (1)
DO(IO1)	Serial Data Output(Data input output 1) (1)
CS#	Chip Enable
WP#(IO2)(3)	Write Protect (Data input output 2) (2)
HOLD# / RESET#(3)(IO3)	Hold or Reset input(Data input output 3) (2)
V_{CC}	Power Supply (2.3-3.6V)
GND	Ground

Notes:
(1) IO0 and IO1 are used for Standard and Dual SPI instructions.
(2) IO0 ² IO3 are used for QUAD SPI / QPI instructions.
(3) WP# and HOLD# / RESET# functions are only available for Standard and Dual SPI.

4.1. Serial Data Input (DI) / IO0

The SPI Serial Data Input (DI) pin is used to transfer data serially into the device. It receives instructions, address and data to be programmed. Data is latched on the rising edge of the Serial Clock (CLK) input pin. The DI pin becomes IO0 - an input and output during Dual and Quad commands for receiving instructions, address, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

4.2. Serial Data Output (DO) / IO1

The SPI Serial Data Output (DO) pin is used to transfer data serially out of the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin. DO becomes IO1 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as

ZBIT CONFIDENTIAL

4.5. Wr 3\ ^ì

ZBIT CONFIDENTIAL

5.2.1 Security Register 0

ZBIT CONFIDENTIAL

5.2.3 SFDP Header Field Definitions

Table 5.3 SFDP Header

SFDP Byte Address	SFDP Dword Name	Data	Description
00h	SFDP Header 1st DWORD	53h	This is the entry point for Read SFDP (5Ah) command i.e. location zero within SFDP space $ 6 & , , ³ 6 ´
01h		46h	$ 6 & , , ³) ´
02h		44h	$ 6 & , , ³ ' ´
03h		50h	$ 6 & , , ³ 3 ´
04h		06h	SFDP Minor Revision (06h = JEDEC JESD216 Revision B) ± This revision is backward compatible with all prior minor revisions. Minor revisions are changes that define previously reserved fields, add fields to the end, or that clarify definitions of existing fields. Increments of the minor revision value indicate that previously reserved parameter fields may have been assigned a new definition or entire Dwords may have been added to the psiot6(e)4(a)3du p p 4(a)4(d)t5(t)-5(79(e)4(n)6( )9(s-5(79(ue)4(d)4( )-3
	SFDP Header 2nd DWORD		

ZBIT CONFIDENTIAL

5.2.4 JEDEC SFDP Basic SPI Flash Parameter

Table 5.4 Basic SPI Flash Parameter, JEDEC SFDP Rev B (Sheet 1 of 5)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
			Start of SFDP JEDEC parameter Bits 7:5 = unused = 111b
30h		E5h	
	JEDEC Basic Flash Parameter Dword-1		

ZBIT CONFIDENTIAL

ZBT CONFIDENTIAL

Table 5.4 Basic SPI Flash Parameter, JEDEC SFDP Rev B (Sheet 5 of 5)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
6Ch	JEDEC Basic Flash Parameter Dword-16	E8h	Bits 31:24 = Enter 4-Byte Addressing = xxxx_xxx1b:issue instruction B7 (preceding write enable not required + xx1x_xxxxb: Supports dedicated 4-byte address instruction set. Consult vendor data sheet for the instruction set definition or look for 4-byte Address Parameter Table. + 1xxx_xxxxb: Reserved = 10000000b not supported Bits 23:14 = Exit 4-byte Addressing = xx_xxxx_xxx1b:issue instruction E9h to exit 4-byte address mode (Write enable instruction 06h is not required) + xx_xx1x_xxxxb: Hardware reset + xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) + xx_1xxx_xxxxb: Power cycle + x1_xxxx_xxxxb: Reserved + 1x_xxxx_xxxxb: Reserved = 11_0000_0000b not supported Bits 13:8 = Soft Reset and Rescue Sequence Support = x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1,2, or 4 wires depending on the device operating mode + 1x_xxxxb: exit 0-4-4 mode is required prior to other reset sequences above if the device may be operating in this mode. = 11_0000b Bit 7 = RFU = 1 Bits 6:0 = Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1 = xxx_1xxxb: Non-Volatile/Volatile status register 1 powers-up to last written value in the nonvolatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register. + x1x_xxxxb: Reserved + 1xx_xxxxb: Reserved = 1101000b Binary Fields: 10000000-1100000000-110000-1-1101000 Nibble Format: 1000_0000_1100_0000_0011_0000_1110_1000 Hex Format: 80_C0_30_E8
6Dh		30h	
6Eh		C0h	
6Fh		80h	

ZBIT CONFIDENTIAL

6.2. Status Register

The Read and Write Status Registers commands can be used to provide status and control of the flash memory device.

Status Register-1 (SR1) and Status Register-2 (SR2) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, and Erase / Program Suspend status.

SR1 and SR2 contain non-volatile bits in locations SR1[7:2] and SR2[6:3], SR2[1] that control sector protection, OTP Register Protection, Status Register Protection, and Quad mode. Bits located in SR2[7], SR1[1], and SR1[0] are read only volatile bits for suspend, write enable, and busy status. These are updated by the memory control logic. The SR1[1] write enable bit is set only by the Write Enable (06h) command and cleared by the memory control logic when an embedded operation is completed.

ctfon Write access to the non-volatile Status Register bits is controlled by the state of the non-volatile Status Register Protect bits SR1[7] and SR2[0] (SRP0, SRP1), the Write Enable command (06h) preceding a Write Status Registers command, and while Quad mode is not enabled, the WP# pin.

A volatile version of bits SR2[6], SR2[1], and SR1[7:2] that control sector protection and Quad Mode is used to control the behavior of these features after power up. During power up or software reset, these volatile bits are loaded from the non-volatile version of the Status Register bits. The Write Enable for Volatile Status Register-32(861(S)-7(R2-5(t)4(en2(c)-5(om)-20(m)-21 an)4(d)45[(c)-5(an)4( )-46(be)4( )-46(us)-3(e)-9(d)-45(to)-5

protection scoms ickyw(i)5(hpo)-7uatwaihing 152(f)-10(or 170(th)-8(eto)-7(y)18pa)-9(i)5csal(no)4(n)] T

c)-6(dg)-7(i)5ngn)-7( )-34a mWrite Stat Registers command man,g andthl WP# n whileQuad

and memory

le for Volatile

Status Registe

ZBIT CONFIDENTIAL

st B[3:1] is Sec42.6urity logic42.6ked. LB[3:1] ca429(n)27(b429(e)27(s)-5(et)28(t)-10(o)27(1429( )256i)5(n429(di)-4(v)6(i)-
7 L P H 3 U R J U D P P D E ƒ À H ° 7 3 ƒ Å ø * P H L€ q ` e 7 €VP H

(R) 9 7 E S # (f S) - 7 u n n c

S # . , (r - 8 4 , t - 4 . H O c 4 - 1 7

yphrm (an)4en

ZBIT CONFIDENTIAL



ZBT CONFIDENTIAL

ZBIT CON

ZBT CONF

ZBT CONCEPT

ZBT CONFIDENTIAL

Table 7.1 Command Set (Configuration, Status, Erase, Program Instructions (1), SPI Mode)

Command Name	BYTE 1 (Instruction)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Status Register-1	05h	SR1[7:0](2)				

ZBIT CONFIDENTIAL

Table 7.2 Command Set (Read Instructions [1], SPI Mode)

Command Name	BYTE 1 (Instruction)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6

ZBIT CONFIDENTIAL

7.1 Configuration and Status Commands

7.1.1 Read Status Register (05h /35h/15h)

The Read Status Register commands allow the 8-bit Status Registers to be read. The command is entered by G U L Y L Q J & 6 O R Z D Q G V K L I W L Q J W K H L Q V W U X F W L R Q I R O O R Z H G E \ W K H Register-2, 3 1 K ´ I R U 6 W D W X V 5 H J L V W H U V 0 R U H D G L Q V W U X F W L R Q V D U H W K H then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.1. The Status Register bits are shown in Section 6.2, Status Registers.

The Read Status Register-1 (05h) command may be used at any time, even during a Program, Erase, or Write Status Registers cycle. This allows the BUSY status bit to be checked to determine when the operation is complete and if the device can accept another command.

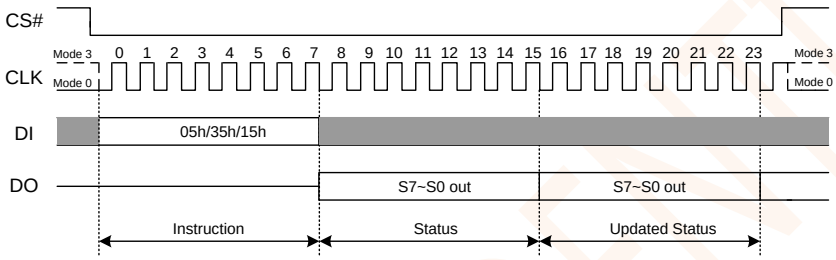


Figure 7.1a Read Status Register Instruction(SPI Mode)

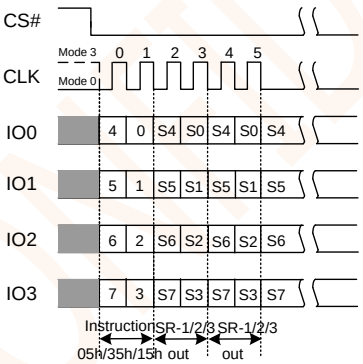


Figure 7.1b Read Status Register Instruction(QPI Mode)

7.1.2 Write Enable (06h)

The Write Enable instruction (Figure 7.2) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving CS# low, shifting the instruction F R G H ³ K ´ L Q W R W K H ' D W D , Q S X W ', S L Q R Q W K H U L V L Q J H G J H R I & / .

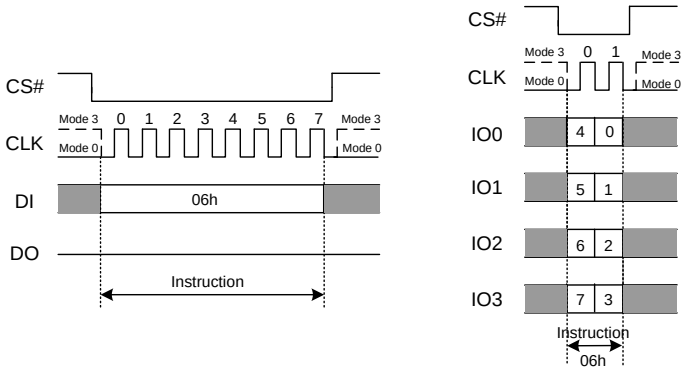


Figure 7.2 Write Enable Instruction(SPI or QPI Mode)

7.1.3 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 6.2 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 7.3) will not set the Write Enable Latch (WEL)bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

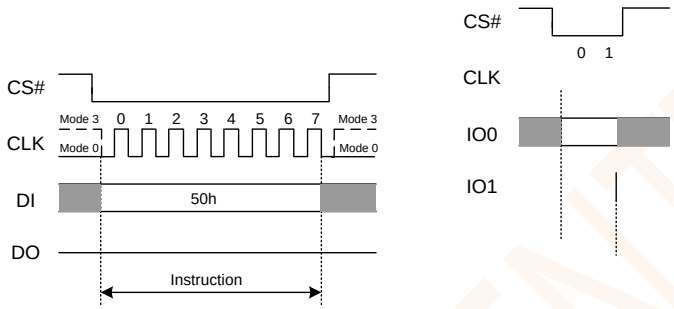


Figure 7.3 Write Enable for Volatile Status Register Instruction(SPI or QPI Mode)

7.1.4 Write Disable (04h)

The Write Disable instruction (Figure 7.4) resets the Write Enable Latch (WEL) bit in the Status Register WR D 7KH :ULWH 'LVDEOH LQVWUXFWLRQ LV HQWHUHG E\ GULYLQJ &6 DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

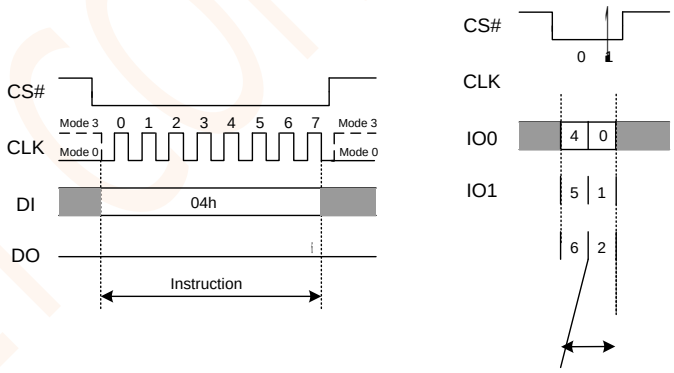


Figure 7.4 Write Disable Instruction(SPI or QPI Mode)

7.1.5 Write Status Register (01h /31h/11h)

Status Regist ypleti--15(hi)7(s)-5( )] TJ ET EMC /P <<>> BDC BT 1 0 0 1150.09462.31am quEs

ZBT CONFID

Register-1, WEL=1). The instruction is initiated by driving the CS# pin low then shifting the instruction code "32h" followed by a 24-bit address (A23-0) and at least one data byte, into the IO pins. The CS# pin must be held low for entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instructions sequence is shown in Figure 7.7.

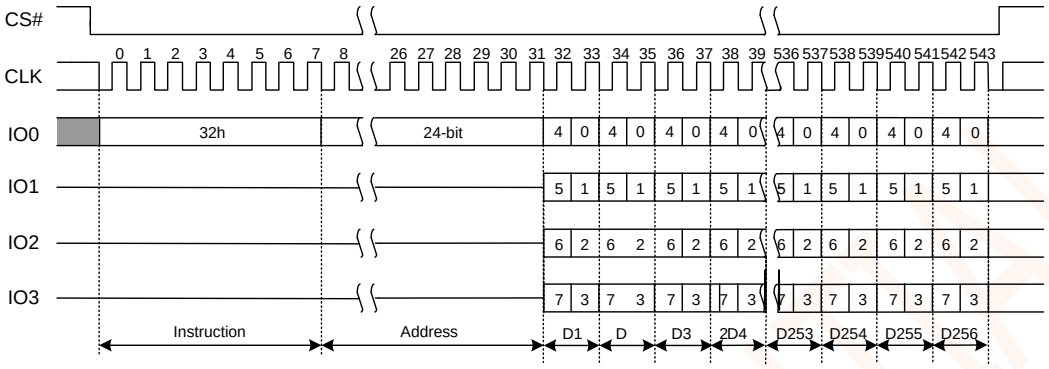


Figure 7.7 Quad Page Program Instruction

7.2.3 Sector Erase (SE) (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and V K L I W L Q J W K H L Q V W U X F W L R Q F R G H ? K (A23-0). The Sector Erase instruction sequence is shown in Figure 7.8.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit.

ZBIT CONFIDENTIAL

ZBIT SEMI

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code ³& K´ RU ³ K´ 7KH &KLS (UDVH LQVWUXFWLRQ VHTXHQFH LV VKRZQ LQ Figure 7.10. The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

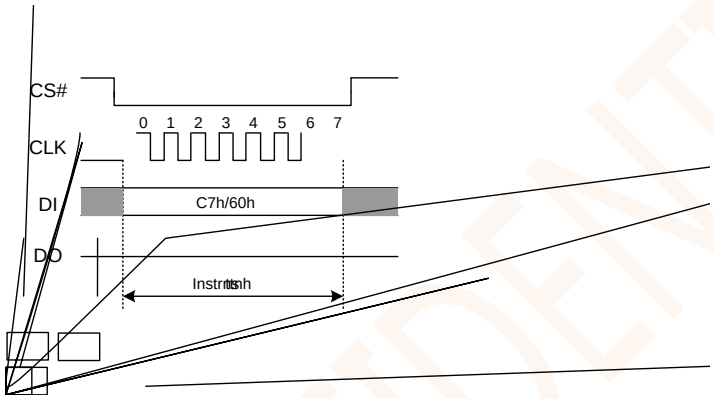


Figure 7.10 Chip Erase Instruction(SPI or QPI Mode)

7.2.6 Erase / Program Suspend (75h)

The Erase / Program Suspend command allows the system to interrupt a Sector or Block Erase operation, then read from or program data to any other sector. The Erase / Program Suspend command also allows the system to interrupt a Page Program operation and then read from any other page or erase any other sector or block. The Erase / Program Suspend command sequence is shown in Figure 7.11.

The Write Status Registers command (01h, 31h, 11h), and Erase commands (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend command is ignored. The Write Status Registers command (01h, 31h), and Program commands (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid during the Page Program or Quad Page Program operation.

The Erase / Program Suspend command 75h will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend command will be ignored by the device. Program or Erase command for the sector that is being suspended will be ignored.

A maximum of time of t_{SUS} (Section 8.5, AC Electrical Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within t_{SUS} and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend command 75h is not issued earlier than a minimum of time of t_{SUS} following the preceding Resume command 7Ah.

Unexpected power off during the Erase / Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques to prevent accidental power interruption, provide non-volatile tracking of in process program or erase commands, and preserve data integrity by evaluating the non-volatile program or erase tracking information during each system power up in order to stoy and repair (r e-erase and re-program) any improperly tinated program or erase operations.

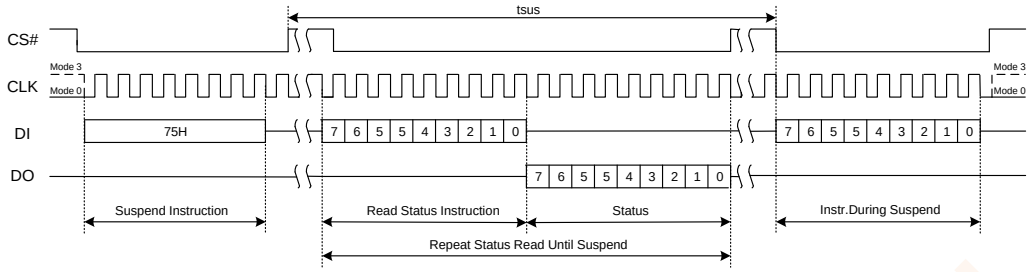


Figure 7.11a Erase / Program Suspend Instruction(SPI Mode)

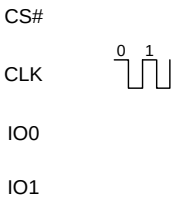


Figure 7.11b Erase / Program Suspend Instruction(QPI Mode)

7.2.7 Erase / Program Resume (7Ah)

7KH (UDVH 3URJUDP 5HVXPH FRPPDQG ³$K´ PXVW EH ZULWWHQ W
RSHUDWLRQ RU WKH 3DJH 3URJUDP RSHUDWLRQ DIWHU DQ (UDVH 3UI
will be accepted by the deU5 tr A >~ì edC BT ET EU> B2 E10(ed)4( )BT tET 4

ZBIT CONFIDENTIAL

24-

ZBIT CONFIDENTIAL

ZBIT CONFIDENTIAL

ZBLCONF

ZBIT CONFIDENTIAL

Z L W K ³ : U D S $ U R X Q G ´ I H D W X U H 7-5 H Standard SPI mode is still valid in QPI mode and can also be re- F R Q I L J X U H G E \ ³ 6 H W 5 H D G 3 D U D P H W H U 7.5.12 and 7.5.13 for details.

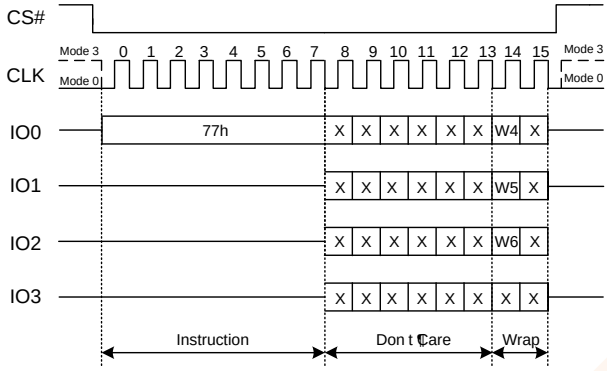


Figure 7.25

ZBIT CONFIDENTIAL

and will not have any effects on the current cycle.

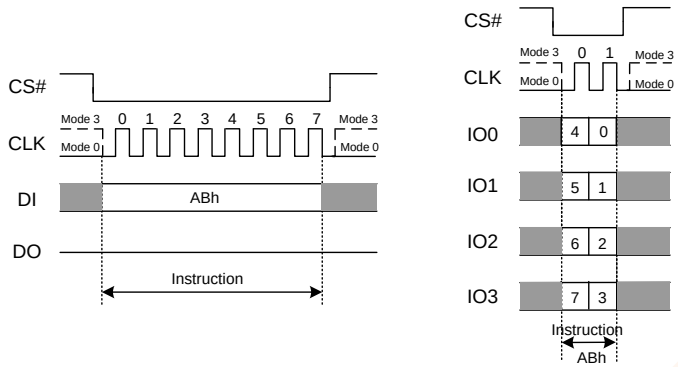


Figure 7.28 Release Power-down Instruction(SPI and QPI Mode)

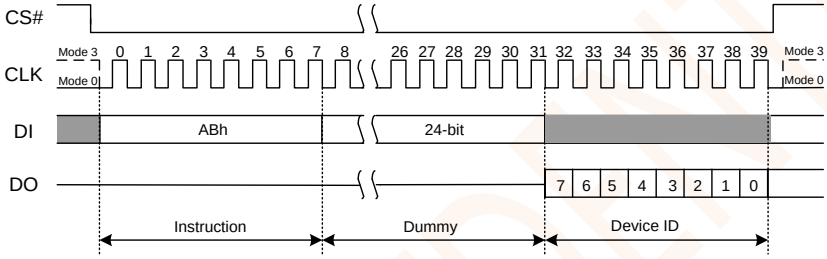


Figure 7.29a Release Power-down / Device ID(SPI Mode)

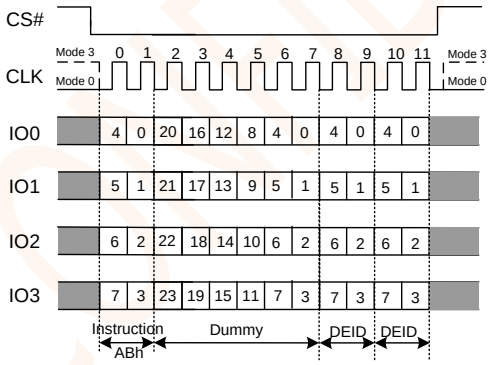


Figure 7.29b Release Power-down / Device ID(QPI Mode)

7.5.3 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.30. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving CS# high.

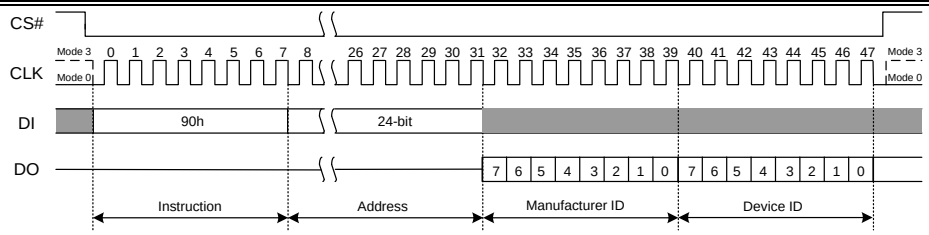


Figure 7.30a Read Manufacturer/Device ID(SPI Mode)

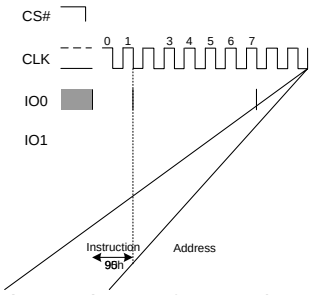


Figure 7.30b Read Manufacturer/Device ID(QPI Mode)

7.5.4 Read Identification (RDID) (9Fh)

For compatibility reasons, the ZB25VQ128 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

7KH LQVWUXFWLRQ LV LQLWLDWHG E\ GULYLQJ WKH &6 SLQ ORZ DQ assigned Manufacturer ID byte and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.31. For memory type and capacity values, refer to Manufacturer and Device Identification table.

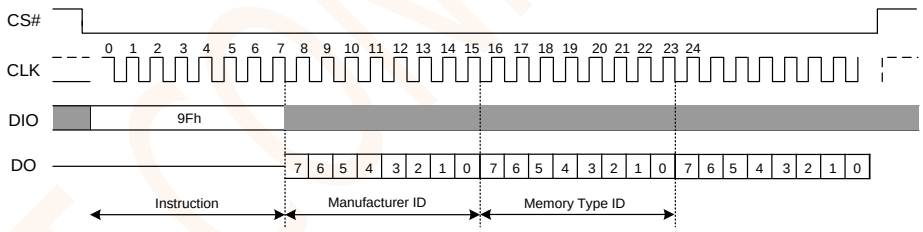


Figure 7.31a Read JEDEC ID(SPI Mode)

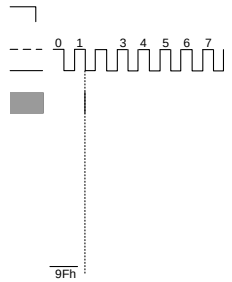


Figure 7.31b Read JEDEC ID(QPI Mode)

7.5.5 Read SFDP Register (5Ah)

7KH 5HDG 6)'3 FRPPDQG LV LQLWLDWHG E\ GULYLQJ WKH &6 SLQ OR followed by a 24-bit address (A23-A0) in WR WKH ', SLQ (LJKW ³GXPP\´ FORFNV DUH D



ZBT CONFIDENTIAL

Address	A23-16	A15-8	A7-0
Security Register-1	00h	10h	Byte Address
Security Register-2	00h	20h	Byte Address
Security Register-3	00h	30h	Byte Address

Note:
1. Addresses outside the ranges in the table have undefined results.

The Program Security Register command sequence is shown in Figure 7.34. The Security Register Lock Bits (LB3:1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, and a Program Security Register command to that register will be ignored.

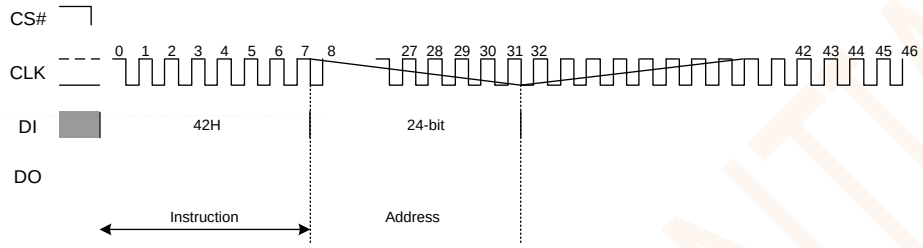


Figure 7.34 Program Security Registers Instruction

7.5.8 Read Security Registers (48h)

The Read Security Register command is similar to the Fast Read command and allows one or more data bytes to be sequentially read from one of the three security registers. The command is initiated by driving the &6 SLQ ORZ DQG WKHQ VKLIWLQJ WKH LQVWUXFWLRQ ³ Bit address (A23-A0) and eight K´ IROC ³GXPP\´ FORFNV LQWR WKH ', SLQ 7KH FRGH DQG DGGUHVV ELWV DUH C the address is received, and following the eight dummy cycles, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. Locations with address bits A23-A16 not equal to zero, have undefined data. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte

ZBIT CONFIDENTIAL

set to 1. If WPS=0, the write protection will be determined by the combinat3(m) c 2L of CMP, SEC, TB, BP2:0 bits in the Status Reg3(m)st The Individual Block/Sector Lock bits are volat3(m)le bits. The defaul values after device

ZBIT CONFIDENTIAL

ZBIT CONFIDENT

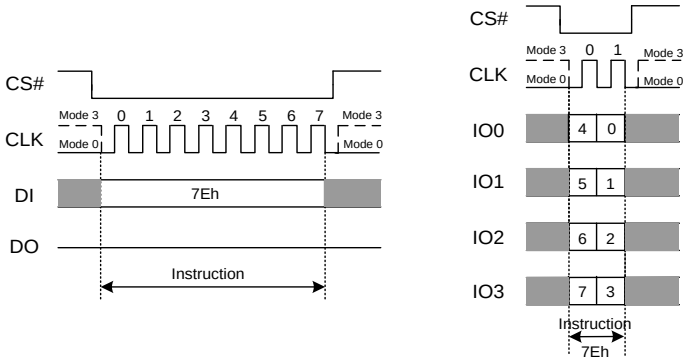


Figure 7.39 Global Block Lock Instruction(SPI or QPI Mode)

7.5.13 Global Block/Sector Unlock (98h)

All Block/Sector Lock bits can be set to 0 by the Global Block/Sector Unlock instruction. The command must be issued by driving CS# low, shifting the instruction code ´98h´into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high. A Write Enable instruction must be executed before the device will accept the Global Block/Sector Unlock Instruction (Status Register bit WEL= 1).

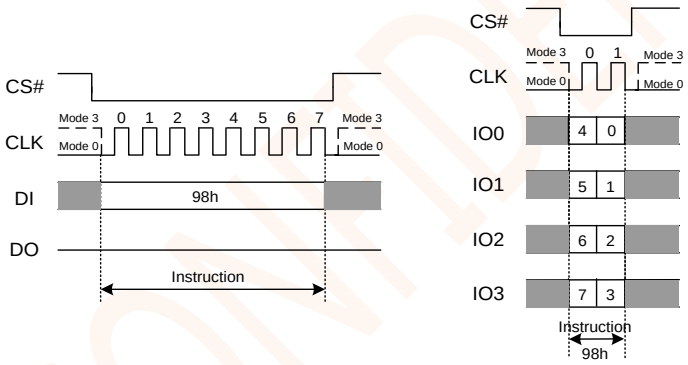


Figure 7.40 Global Block Lock Instruction(SPI or QPI Mode)

7.5.14 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the CS# S L Q O R Z D Q G V K L I W L Q J W K H L Q V W U X F W L R C 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most instio4(ID o)14 Tm-17( )-58(bi)7(t)1 l143l (D3 A(ns)-38(tir)4(r)-3(eo)14(s)-46(Ft)1are w53(,)-9Ftal-7(tF78 Tmm [(

ZBT CO



ZBT CONFIDENTIAL

The ZB25VQ128 support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. ³(QWHU 43, K´LQVWUXFWLRQ LV WKH RQO\ ZD\ WR VZLWFK WKH GHYLFH IURP 63

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of ZBIT serial flash memories. See Instruction Set Table 7.1-7.4 for all supported SPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register- PXVW EH VHW WR ILUVW DQG DQ ³(QWHU 43 the Quad K´LQVW (QDEOH 4(ELW LV WKH ³(QWHU 43, K´LQVWUXFWLRQ ZLOO EH LJ See Instruction Set Table 7.5 for all the commands supported in QPI mode. When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

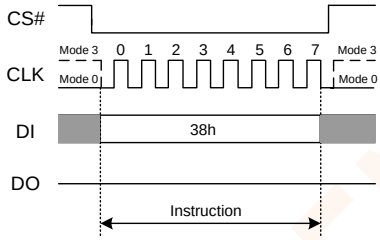


Figure 7.46 Enter QPI Instruction (SPI Mode only)

7.5.20 Exit QPI Mode (FFh)

In order to exit the QPI mode and return WR WKH 6WDQGDUG 'XDO 4XDG 63, PRGH instruction must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

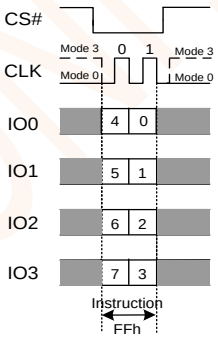


Figure 7.47 Exit QPI Instruction (QPI Mode only)

ZBIT CONFIDENTIAL

8. ELECTRICAEn5E7t2(CTERIS2(LET)-9TJ ET EMC /P <<>> BDC BT 1 0 0 1 695.61 601.

ZBIT CONFIDENTIAL

ZBT